Remarks

Claims 1-8 are currently pending in this application. No claim amendments are introduced.

The Examiner rejected applicants' claims 1-8, stating that the claims are obvious under 35 USC § 103(a). The Examiner cited US Patent No. 6,281,535 to Ma et al. (Ma et al. hereinafter) in view of US Patent No. 5,471,418 to Tanigawa (Tanigawa hereinafter) as the basis for the rejection.

Applicants' invention is an integrated circuit that consists of a semiconductor substrate with semiconductor devices formed therein and thereon, a first wiring layer located over the substrate, a second wiring layer located on the first wiring layer, and a capacitor. The capacitor has metal-based charge-storage electrodes that extend through the entire thickness of the second wiring layer and at least part of the first wiring layer. The wiring layers have interconnect wire embedded therein.

Referring to Figure 1A of applicants' specification, there the applicants illustrate a portion of one integrated circuit (IC) 8. The IC 8 includes a semiconductor substrate 10, semiconductor devices 16, 18 located on the substrate 10, and a protective dielectric layer 14 covering both the semiconductor devices 16, 18 and the substrate 10. Exemplary semiconductor devices 16, 18 include transistors, diodes, and resistors. The IC 8 also includes multiple wiring layers 11-13 located on the layer 14, and an inter-wiring-layer capacitor 20 stacked over the protective layer 14. The inter-wiring-layer capacitor 20 extends through more than one of the wiring layers 12-13. The inter-wiring-layer capacitor 20 is completely disposed in a window formed in the wiring layers 12 and 13.

Ma et al. describes a device in which the capacitor is formed in a single wiring layer. Referring to FIG. 18 of Ma et al., it is abundantly clear that the capacitor is formed in dielectric layer 38 only and not "through the thickness of one wiring layer and in a portion of another wiring layer" as required by applicants' claim 1. The Examiner appreciates this difference, but states that Tanigawa makes it obvious to modify the capacitor described in Ma et al. by having it extend through the thickness of a second wiring layer in order to increase its capacitance. The applicants respectfully disagree.

Applicants' claims require that the capacitor be disposed completely within the window. Referring to FIG. 3 of Tanigawa, the capacitor is clearly not completely disposed in

a window formed in insulating layers 6, 8 and 10. The polysilicon storage electrode 11, dielectric layer 12 and opposite electrode 13 are all partially disposed outside the window formed in insulators layers 6, 8 and 10. At column 5, lines 48-58, Tanigawa states that the advantage of its DRAM cell is the fact that the storage electrode 11, the dielectric 12 and the opposite electrode 13 are provided on the third interlayer insulator 10. According to Tanigawa, this provides an advantage, since the thickness of the storage electrode 11 can be made thicker. Thus, Tanigawa teaches away from the present invention by teaching that it is advantageous to have the capacitor partially outside the window in which the capacitor is formed.

Thus, if one were to modify the capacitor in Ma et al. based on Tanigawa, one would not completely dispose the capacitor in window that extends completely through the thickness of a first wiring layer and through at least a portion of a second wiring layer. One would do what Tanigawa et al. suggests, and form a portion of the capacitor over the dielectric layer. Since Tanigawa et al. desire a thick storage electrode 11 (column 5, line 54), Tanigawa et al. clearly does not suggest forming both the bottom storage electrode 11 and the top electrode (i.e. the cell plate) completely within a window. Therefore the combination of Ma et al. and Tanigawa et al. does not render obvious applicants' invention. It is for these reasons that the applicants respectfully request the Examiner to withdraw his rejection of claims 1-8 as obvious based on Ma et al. in view of Tanigawa et al.

The Examiner believes that he did not employ inappropriate hindsight in combining the teachings of Ma et al. and Tanigawa in order to form the present rejection. The Examiner insists that his hindsight reasoning takes into account only the ordinary skill at the time of the claimed invention. The Examiner concludes that, as such, his reconstruction of the teachings in Tanigawa are appropriate in order to combine with Ma et al. to render the present invention obvious.

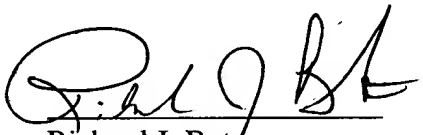
The applicants strenuously disagree. Tanigawa et al. provides an express teaching. That teaching, forming a portion of the capacitor over the dielectric layer, precludes a combination with Ma et al. to render the present invention obvious. The Examiner has not shown the requisite motivation to combine. That is, if there was motivation to combine, what provided the motivation to ignore Tanigawa et al.'s express instruction to form the capacitor over the dielectric layer? There is no such instruction or suggestion provided from Ma et al.

Ma et al. teaches the formation of the capacitor in one wiring layer. Ma et al. does not teach the formation of the capacitor through multiple layers. Tanigawa et al. provides the suggestion to form the capacitor through multiple layers, but in doing so, expressly instructs one skilled in the art to form a portion on the dielectric surface. Thus, the only way one skilled in the art would combine Tanigawa et al. and Ma et al. to arrive at the present invention is to work backwards from the present invention. Based upon the fact that the present obviousness rejection is based on inappropriate hindsight, applicants respectfully request the Examiner to withdraw his obviousness rejection.

In view of the foregoing arguments and amendments, applicants submit that their claims are in condition for allowance. Favorable action is respectfully requested.

Respectfully submitted,

Philip W. Diodato
Chun-Ting Liu
Ruichen Liu



Richard J. Botos
Reg. No. 32,016
(610) 712-8520

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Docket Administrator
Agere Systems Inc.
Four Connell Drive
Room 4U533C
Berkeley Heights, NJ 07922